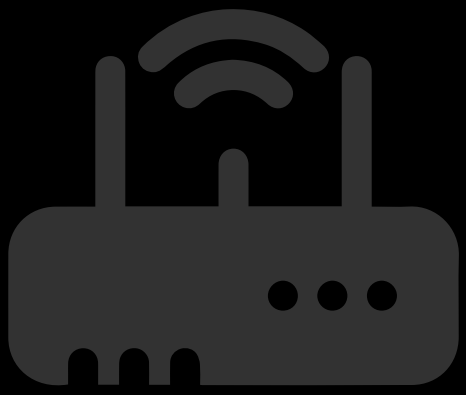
CONNECTIVITY SoC – RTL TO GDS II

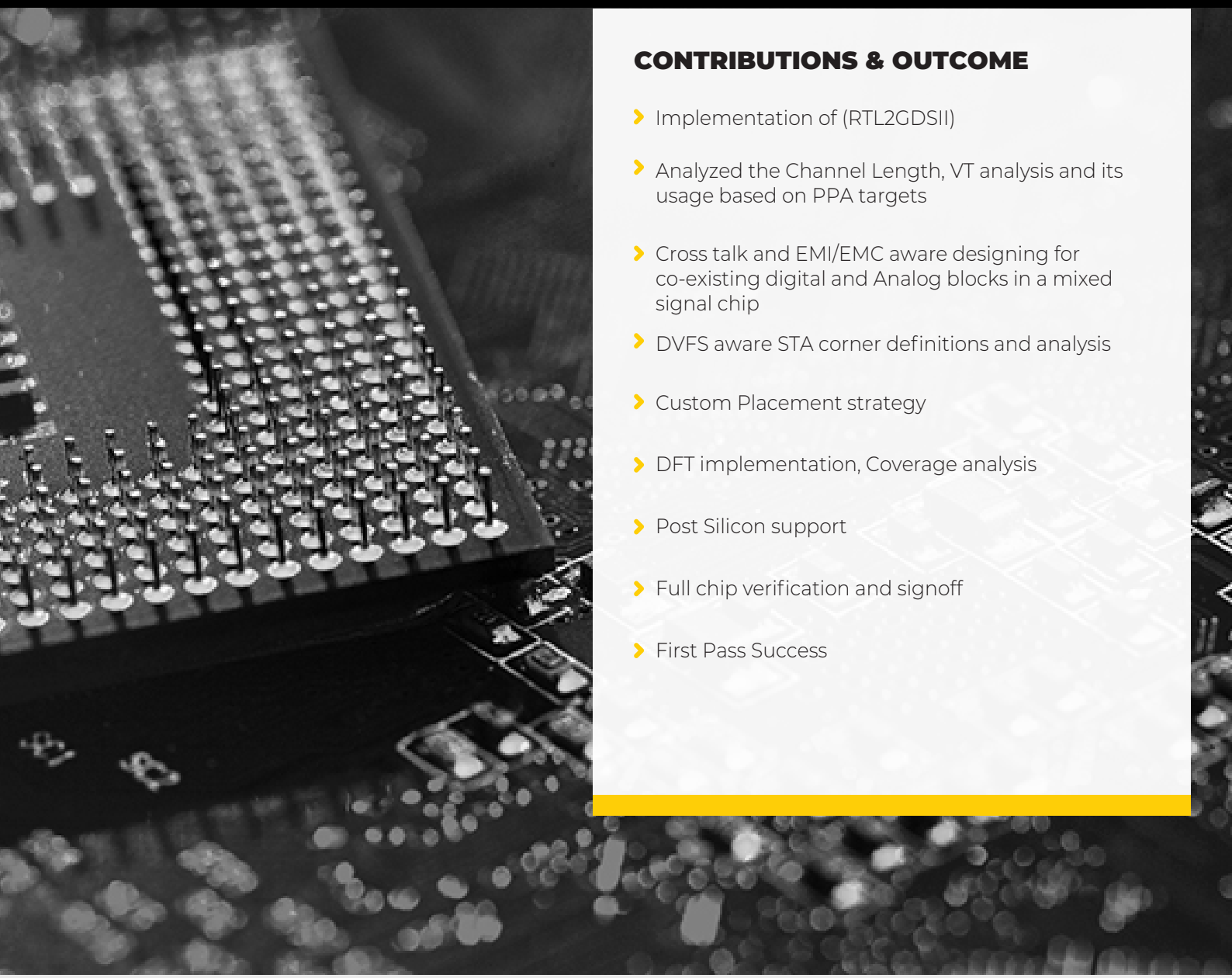
OVERVIEW

The customer is a Tier-1 Semiconductor Company and wanted a partner for Connectivity SoC derivative.

DESIGN FEATURE & CHALLENGES

1. WiFi & BT chip with high density, dynamic power transmission
2. Low tech process, low power for versatile applications
3. Industry leading microcontrollers at industry benchmark speeds for high performance applications
4. Peripherals: PCIE, SDIO, UART, I2C, SPI, PCM, I2S, JTAG covering industrial, consumer, networking use cases
5. PPA Optimization
6. Complex Low Power State Machine Verification





CONTRIBUTIONS & OUTCOME

- Implementation of (RTL2GDSII)
- Analyzed the Channel Length, VT analysis and its usage based on PPA targets
- Cross talk and EMI/EMC aware designing for co-existing digital and Analog blocks in a mixed signal chip
- DVFS aware STA corner definitions and analysis
- Custom Placement strategy
- DFT implementation, Coverage analysis
- Post Silicon support
- Full chip verification and signoff
- First Pass Success

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