GDDR6 TEST CHIP

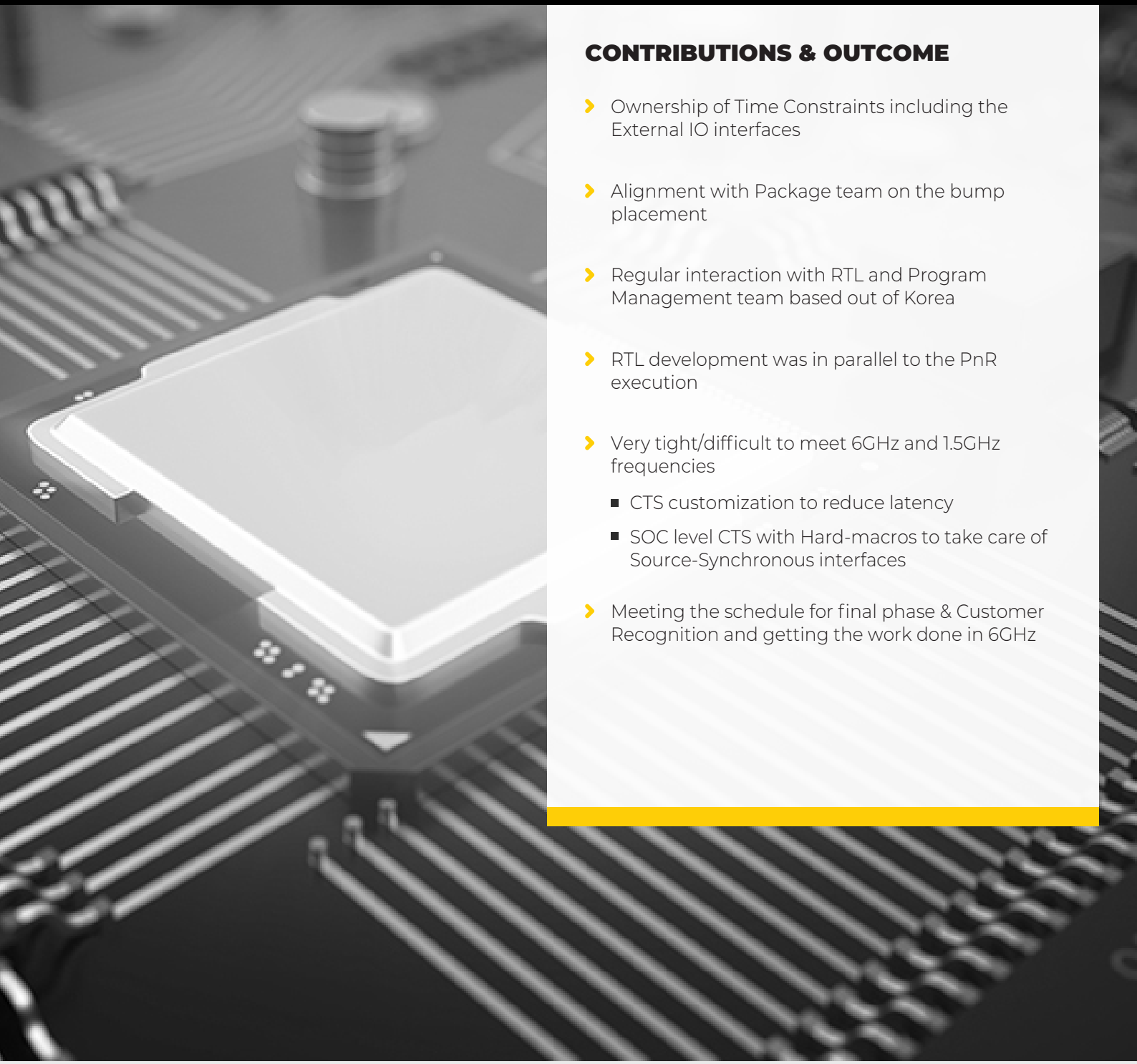
OVERVIEW

The customer is one of the top electronic equipment manufacturers. They wanted to test graphic chip (GDDR6) to enhance the performance of the chip.

DESIGN FEATURE

It was a complex project as this involved the first ever GDDR6 chip test using 8LPP technology. With additional requirements like:

1. IP Max frequency of 6GHz and controller frequency of 1.5GHz
2. Hierarchical based implementation with SOC and multiple Hard-macros
3. Each block having >1 million instances



CONTRIBUTIONS & OUTCOME

- Ownership of Time Constraints including the External IO interfaces
- Alignment with Package team on the bump placement
- Regular interaction with RTL and Program Management team based out of Korea
- RTL development was in parallel to the PnR execution
- Very tight/difficult to meet 6GHz and 1.5GHz frequencies
  - CTS customization to reduce latency
  - SOC level CTS with Hard-macros to take care of Source-Synchronous interfaces
- Meeting the schedule for final phase & Customer Recognition and getting the work done in 6GHz

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