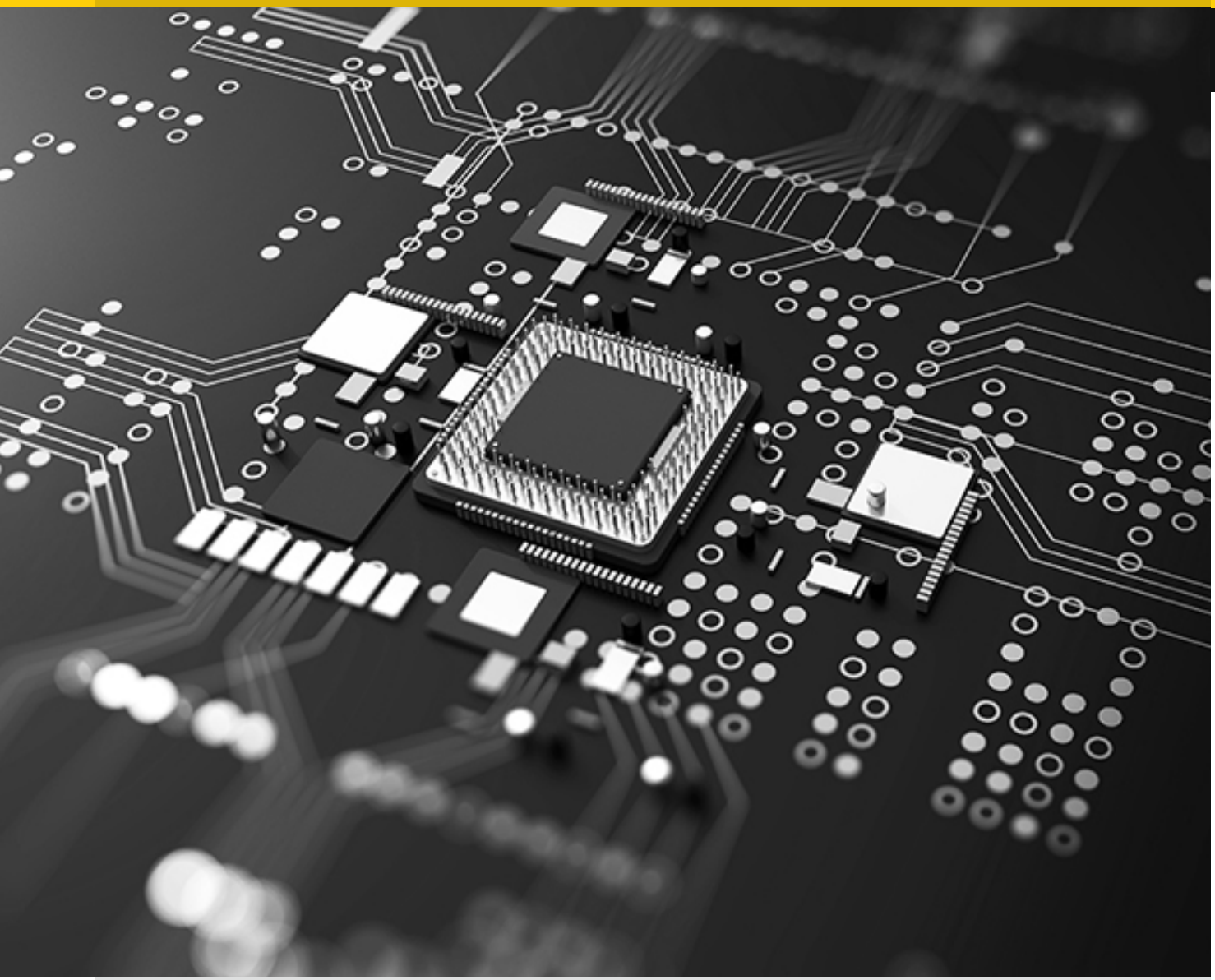
SERDES CHIPS



OVERVIEW

The customer required Design, IP Verification, Fullchip verification, Synthesis & DFT on several high speed SERDES chips in turnkey mode.

CHALLENGES

1. Agile project management with very short cycle time (spec to TO in ~6 months), milestone based project assessment
2. Using 65nm technology process
3. Project Execution and Management from Test Planning through Closure
4. SOC Bring Up

SOLUTION

IPDV

- IP level verification for DisplayPort Rx & DisplayPort Tx
- Bridging gaps between 3rd party IP, another 3rd party VIP, client's RTL, our testbench and maintaining versions of the same
- Bringing up complex modes in a very short time

ChipDV

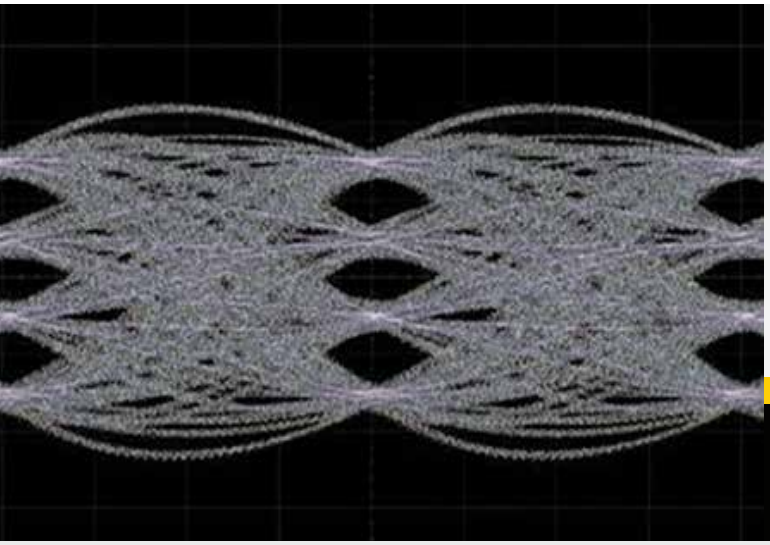
- Chip level verification for 3 SERDES chips with different chip options
- Involved DP1.4, FPD3, FPD4, SPI, I2C, I2S interfaces
- Bringing up of complex applications, including daisy chaining different chips in various stages of development
- Gate level simulations

Synthesis, DFT

- Fullchip synthesis ownership on 2 chips
- Constraints dev, synthesis scripts, synthesis & ECOs
- LEC: RTL to NL, NL to NL
- Fullchip DFT architecture on 3 chips, including scan & Mbist arch

Design, RTL

- Microarchitecture & RTL for pattern generator, checker, timing control, eFuse, Link BIST, Analog test modes, pin straps, etc
- Clock & reset control
- Lint, CDC, LEC across multiple versions



OUTCOME

- Timely delivery of the project
- Working with remote client design team

To know more about how ACL can partner with you to help create Digital Transformation, connect with: **business@acldigital.com**

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