5G RADIO ASICS

IP Development, Verification, Emulation and Top-level Verification of complex ASICs

Service: 5G

OVERVIEW

The Client is a leading multinational networking equipment manufacturer involved in design & development of 5G Radio ASICs. Our Semiconductor practice team contributed in the development of multiple components of 5G Radio ASICs. This includes IP Development (Ethernet, CPRI, RFIC Control & Digital Interfaces), Radio IO Control systems, 5G SoC ASIC Front end, RF ASIC Integration and Emulation of Radio Baseband.

High-performance teams were created to collaborate and work together with our customer's team in a well-structured managed services model.

IP DEVELOPMENT

Key Features

- BEAM FORMING IP to support up to 32 antennas and up to 400Mhz bandwidth which included Narrow Beams, Wide Beams & Tapering support
- POLYPHASE INTERPOLATION Support for Symmetric, Asymmetric filter variants with even and odd number of taps
- POLYPHASE ADAPTER to convert multiple input data streams to polyphase data in the Radio digital front end filter pipes

Challenges

- Complex equations for Antenna calculations and Beamforming calculations
- Time limitation for completing all the Up-Link (UL-32) or Down-Link(DL-32) antennas calculations
- Clock gating to get a higher power save
- Cascaded multiplex symmetrical filter design
- Support for Clock to Sample ratio minimum 1 to N cycles

5G SOC FRONT END

Key Features

- Multiple synchronous clocks, including 12 clocks with Max Frequency of 760MHz
- Instance count of 36million with Hierarchical partitioning (5 hard macros and 1 top level HM)

Challenges

- Flow setup for Synthesis and Timing signoff
- Challenges due to wide and short shape of chip
- High utilization in narrow channels
- Timing constraints development
- Aggressive power targets

ETHERNET IP VERIFICATION

Key Features

- Ethernet for digital baseband transmission (5G)
- 8 ports – 25Gbit/s each ports

Challenges

- System C - TLM based predictor model integration
- Several class of internal/external VIPs and their integration
- Complex SV-UVM verification environment
- Coverage closure with 100% functional & code coverage
- Error Injection (stimulus)

EMULATION OF RADIO BASEBAND

Project Specification

- Instance count of 36 million
- Integrated subsystems for CoreSight debug, CPRI, Filter chain and ARM Cortex Slave processors

Challenges

- Building Emulation database with capacity of 9 domains and palladium PZ1 overcoming synthesis issue related memories and other subblocks of the system
- Bringing up the System level functionality of ARM CoreSight Debug subsystem with Lauterbach Debug Hardware and software, including the basic and advanced features of debug and trace functionality of subsystem through JTAG
- Bringing up of CoreSight debug subsystem test cases on emulation platform in automated way for all the RTL releases from bronze to Gold

VALUE DELIVERED

- Formation of a highly competent team with a broad expertise in 5G ASIC design, verification, SOC emulation and Top-level Verification
- Faster product realization with lower R&D expenditure
- Realization of a complex 5G Radio ASIC on time with better quality and performance

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