RTL TO GDSII FOR A FABLESS SEMICONDUCTOR COMPANY

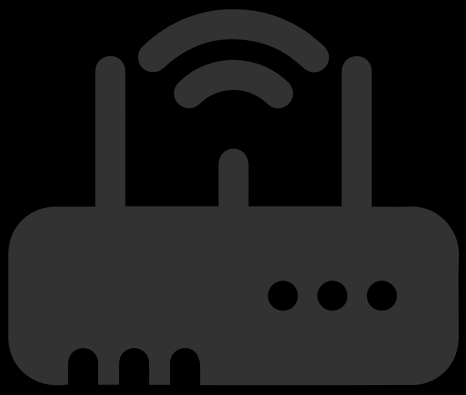
Service: IoT

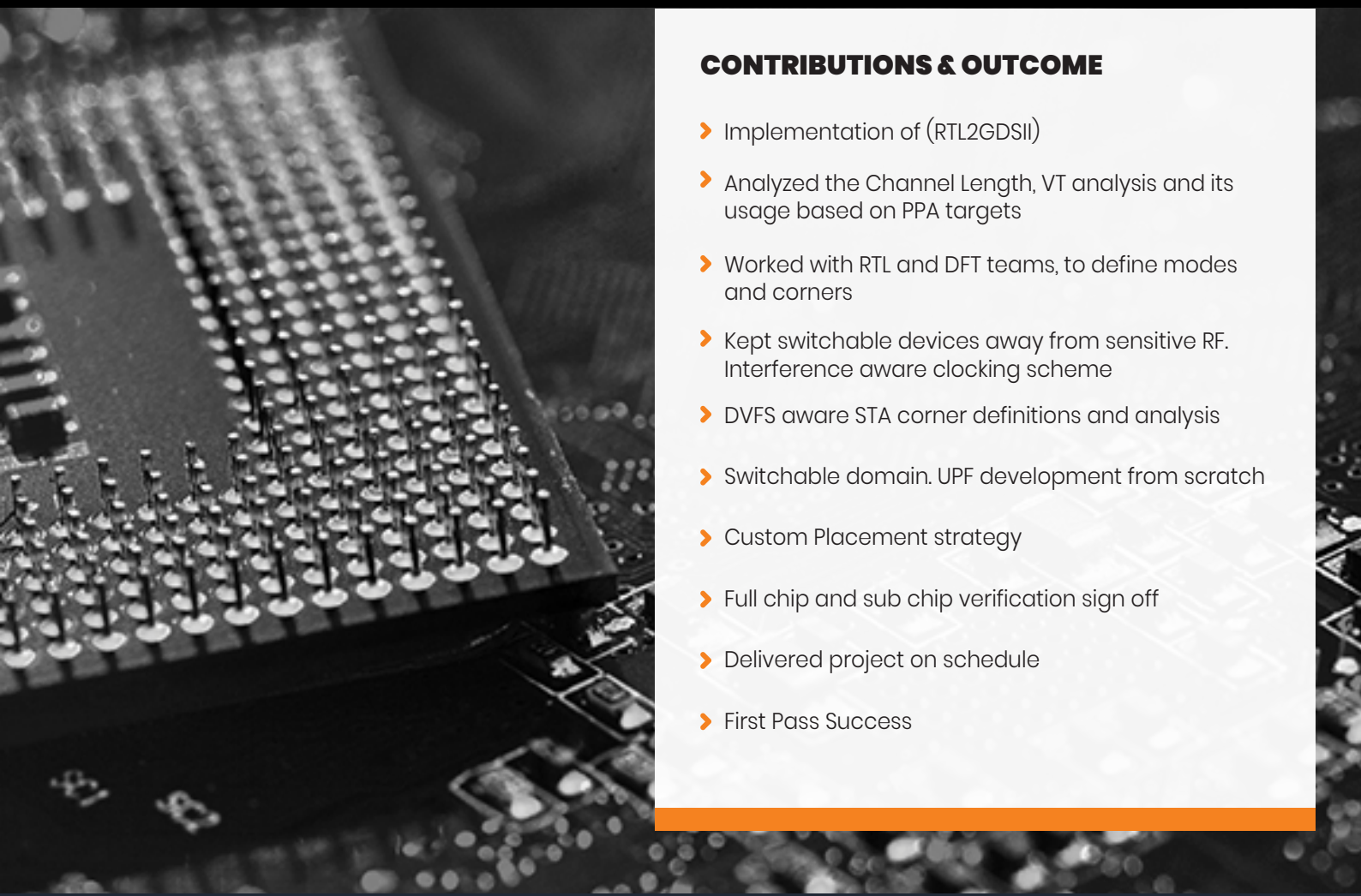
OVERVIEW

The customer is a Fabless Semiconductor Company and wanted a partner for a low power IoT derivative chip.

DESIGN FEATURE & CHALLENGES

1. IP Max frequency of 6GHz and controller frequency of 1.5GHz
2. Mainstream High Performance process node, FPBGA
3. WLAN -960MHz max, ARM CR4 - 360MHz, BT - 96 MHz. DSP – 96MHz
4. Peripherals: PCIE, SMIF, SDIO, UART, I2C, SPI, PCM, I2S, JTAG, SWD and CoEx
5. PPA Optimization
6. RF Co-existence with High Speed Digital
7. Complex Low Power State Machine Verification





CONTRIBUTIONS & OUTCOME

- Implementation of (RTL2GDSII)
- Analyzed the Channel Length, VT analysis and its usage based on PPA targets
- Worked with RTL and DFT teams, to define modes and corners
- Kept switchable devices away from sensitive RF. Interference aware clocking scheme
- DVFS aware STA corner definitions and analysis
- Switchable domain. UPF development from scratch
- Custom Placement strategy
- Full chip and sub chip verification sign off
- Delivered project on schedule
- First Pass Success

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