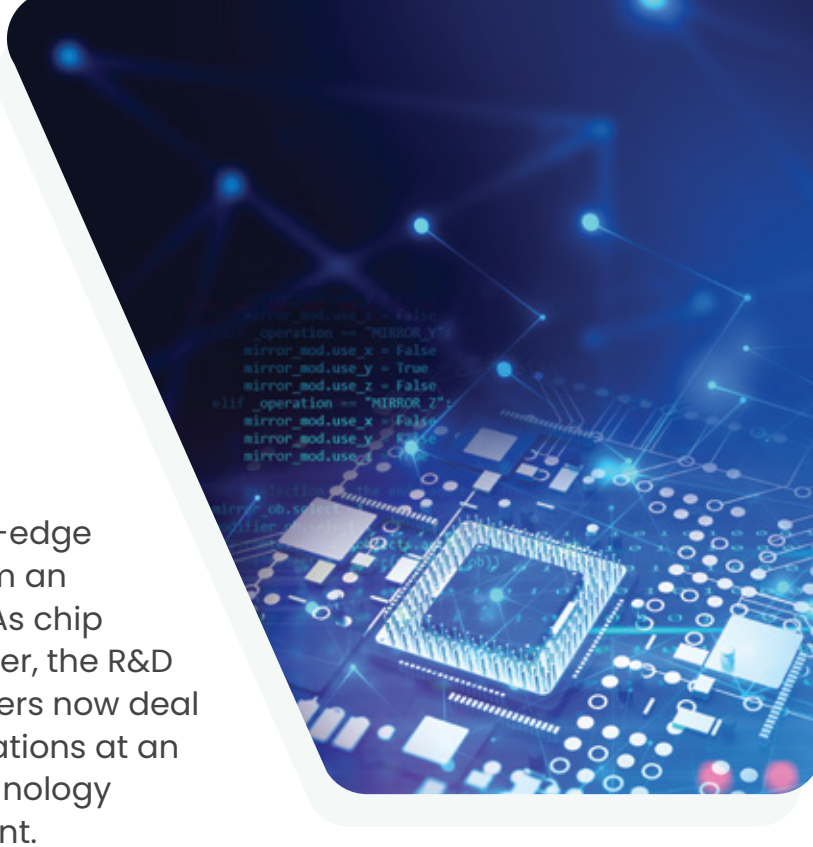
ACL Digital
an ALTEN group company



TSMC Technology Node Expertise

Over the past decade, the need for leading-edge technology leadership has transitioned from an amorphous goal to an absolute necessity. As chip manufacturing technology nodes get smaller, the R&D has become more challenging as researchers now deal with quantum effects due to structural variations at an atomic level, and other manufacturing technology limitations that can complicate development.

ACL Digital Value Offerings

Making the right choices of leading technology nodes and appropriate library usage is the crux of landing the most optimized Power, Performance & Area (PPA) metrics for a design. Leverage ACL Digital's TSMC technology Node Expertise to make that right choice.

Experience in TSMC PDK, Library Technology

- Technology options selection for tradeoff between IP requirements and overall design targets (die size, performance, optimal die partitioning-multi-die if needed)
- Tools for Die size, Power consumption analysis based on IP/process variants

Correct-by-Construction Model-based Domain Specific Expertise/Methodology

- **Automotive:** Redundant architecture, Reliability, Clock tree aging, ISO 26262
- **Networking, Storage:** Partitioning design, placement of various subsystems for performance and utilization optimization, High Speed interfaces (Memory/IO)
- **IoT:** Mixed Signal/RF designs (high speed clocks) interference with Digital/ Processor designs, shielding/isolation, floor plan for substrate noise isolation analysis

Die/Package End-to-End Design

Simulation to ensure design performance in package of choice (FC-BGA, Wirebond MLF, etc.)

Covering a Broad Spectrum of Use Cases including

- Low Power Edge Devices
- High Performance Computing

Market segments we cater to

- **High Performance Computing / AI**
  - RISC V
  - AI / ML
  - Vision Processor
  - GPUs
- **Storage & Networking**
- **Automotive**
  - ADAS
  - Infotainment & Connectivity
- **High Pedigree Start-Ups. (Special Programs for Start-Ups)**

Why ACL Digital?

ACL Digital can be your reliable partner to enable

- Best die size for large gate count designs - optimum die cost
  - *Design optimization with large system IP integrations - Multi-Protocol SerDes*
- Design success: First-time right designs to reduce time to market and development cost
- Best yield in process technology chosen in TSMC
- Improved reliability

ACL Digital's ability to define the design implementation flow from the ground up without a flow from Client

- Benefits start-ups who need help with such designs
- Helps build Libraries, Frequency pushed, Lowest power designs

ACL Digital's high-quality tapeout design flow with the following features

High Quality Tapeout!

Technology Nodes

- 250nm to 28nm (Bulk CMOS)
- 16nm to 7nm (finFET)

Domains

Networking, Storage, Automotive Infotainment, IoT, Servers, Tablets, Mobile Communications

Hardening Skills

- High end Processors (5.5 GHz)
- DSPs
- A9 Core Hardening Experience (Custom flows depending on PPA targets)
- Redundant Cores, in Lock-Step mode
- A9 subsystem hardening with clock synchronicity (1.2GHz)
- DDR3 clocking macro

Full Chip Expertise

- Physical Architects with Multiple Networking & Storage ASIC tapeout experience (of the order of 284mm2)
- 110Mn Gates, 162Mbits of RAM
- 2 Crossbars ; 1.2GHz & 800MHz
- Multiple Quad Cores on Chip
- Upto 9 DSPs on the same device
- Interfaces like DDR3 (1866), SRIO, SGMII, CPRI
- Custom scripts for crosstalk immune staggered buffering and Pipeline register placements

Complex Clocking Architectures

- Clock Mesh, Multipoint CTS H-Tree & Traditional CTS expertise
- Critical Path Aware, Divergence controlled construction
- Custom scripts to check and ensure "RC Balancing" & optimal "Logic Level Balancing" along the entire clock tree

STA flow development & Analysis

- Constraint development from scratch
- IP constraint Integration
- Custom "DMSA aware" ECO scripts
- Custom "Clock QoR" analysis scripts
- Corner definitions and margin flows, based on Architecture Demands
- Experience working with Aging Libraries. A must for Automotive Architectures

Sub System Level Expertise

- Upto 7fF RTL2GDSII ownership
- 1.5Million Gates, 1.2GHz, 200 SRAMs
- Both channel based & abutted floorplan Config
- UPF development from scratch
- Multi-Voltage and switchable domains
- DCT & Placed Gates flow experience
- Special techniques like Relative Placement, Multi-bit flop usage
- Custom scripts for "placement and timing aware logic cloning and restructuring"
- DRC/LVS/ANT/PERC /IR/IVD/EM fix

ACL's "DOMAIN Intelligence BASED" Technology Node, Die Size And Power Estimations

Performance Focused Network Processors

- Route Intensity aware layer stack selections
- Hybrid Partitioning Strategy – Channel and Abutment
- Net Intensive Architectures. Crosstalk aware bus segmentation and net spreading
- "Asynchronous load and mix" aware channel budgets
- "RC Balanced" Datapaths
- Budget aware "slice register" insertion and placement. Scaled into Die-Size estimator
- Mesh, Multi-Point CTS, H-Tree aware die size scaling
- Area estimations on Macro Intensive Partitions. "Access time aware" SRAM packing estimations and channel calculations. Aspect ratio friendly, Block and Muxing options definitions of SRAMs
- Low Power Overhead math. Power Plan Aware Die Sizing
- ECC, Parity aware die-size scaling
- AVS, AVSO, DVFS support
- SRAM Configuration Aware BISR estimations and eFUSE math
- "Dynamic Data Transition" and "Power aware" Standard Cell VT and Channel Length selections
- Bonding and Package Route friendly IO Ring estimations. Challenging Multi-Protocol SerDes, DDR, USB PHY aware floorplans

Power Sensitive IoT

- Power Aware Processor Core and Subsystem Implementations. Intelligent Area Calculations
- "High Cell Utilization Aware" Layer Stack Selections
- Cell utilization stretched to the limits
- "Architecture aware" datapath placement estimations and die scaling
- Intelligent, Physical Partition Planning at die estimation phase itself, to minimize channel wastage
- Leakage, Dynamic Power optimal transition settings and overhead calculations
- Power sensitive, VT and channel length mix. "Frequency Aware" Standard Cell VT, Track and Channel Length selections
- "Substrate Noise aware" halo calculations. RF Integration aware
- Voltage Island aware die scaling
- "Pin Density aware" cell utilization planning. Die size scaled based on "localized complex gate" usage
- Substrate Noise Aware & RC Balanced, traditional CTS strategy. Overhead math based on optimal transition, VT mix
- Leakage Power Aware SRAM selections
- Memory Channel Math, based on access times and channel requirements
- Bonding and Package Route Friendly, IO Ring Estimations. RF IP aware (WiFi, Bluetooth, Zigbee)