FIT Rate Calculations

for FMEDA in ISO 26262

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Abstract & Abbreviations

The amount of safety electronics in vehicles is increasing rapidly. Thus, more and more features need to be developed according to the ISO 26262 standard. The ISO 26262 standard for functional safety talks about various safety analysis techniques. FMEDA is one of the essential safety analysis techniques for hardware design. Failure rates or FIT rates are a significant input for this analysis. This paper will look at various methods of calculating FIT rates with examples.

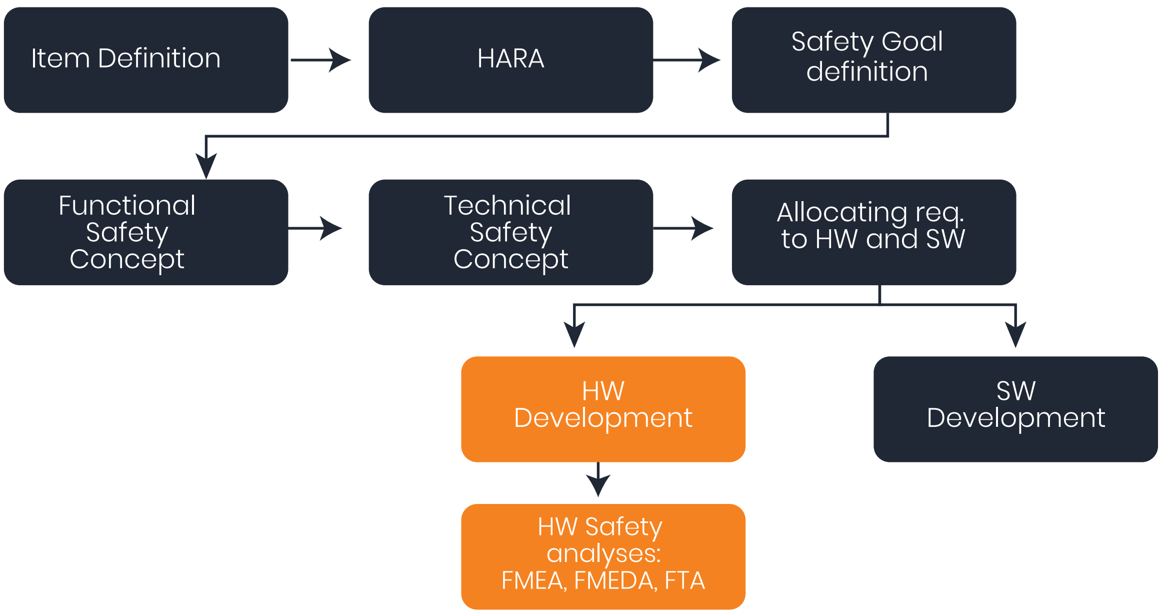
FMEDA	: Failure Mode Effects and Diagnostic Analysis
FIT	: Failure in Time
E/E	: Electrical/Electronics
HW	: Hardware
SW	: Software
SPFM	: Single Point Fault Metrics
LFM	: Laten Fault Metric
ASIL	: Automotive Safety Integrity Level
FMEA	: Failure Mode Effects Analysis
FTA	: Fault Tree Analysis
BOM	: Bill of Material
HTOL	: High Temperature Operational Lifetime
BFR	: Base Fit Rate
EOS	: Electrical Overstress

Introduction

Safety features in today's vehicles are more important than ever before. The newer trends of connected and autonomous vehicles' shared mobility and electrification demand car electronics to be safer and more reliable. Functional safety is a part of the overall safety of a product, which focuses on getting the correct input, processing, and delivering the correct output. In terms of risk, the system should avoid unreasonable risk due to the malfunctioning behavior of E/E systems.

Initially, the automotive industry followed the IEC 61508 standards for functional safety. However, since the automotive industry is very complex and with the distributed development approach, the need was felt to have a dedicated standard for automotive functional safety. The first edition of ISO 26262 was published in 2011. The standard was later updated to address additional concerns regarding motorcycles, Trucks and Buses, and semiconductor device development. Part 11 of ISO 26262 2nd edition focuses on semiconductor IP development in detail.

The latest edition (2018 edition) of the standard has 12 parts. Parts 4, 5, and 6 address the product development at the system, HW, and SW levels. In this paper, we will focus on FMEDA and especially FIT rates calculation which is contained in part 5: Product Development at HW level. One of the critical work products of part 5 is the evaluation of HW architectural metrics (SPFM and LFM). FMEDA is an analysis that helps us calculate these metrics and tells whether our HW design meets the required ASIL level.



Safety Analysis

Part 5 of ISO 26262 provides guidelines for HW requirements, architecture, detailed design, safety analysis, verification, and testing. The safety analysis can be qualitative as well as quantitative. The qualitative analysis includes FMEA, while the quantitative analysis could be FMEDA. FTA can be done as both quantitative and qualitative, and in this paper, we shall focus on FMEDA.

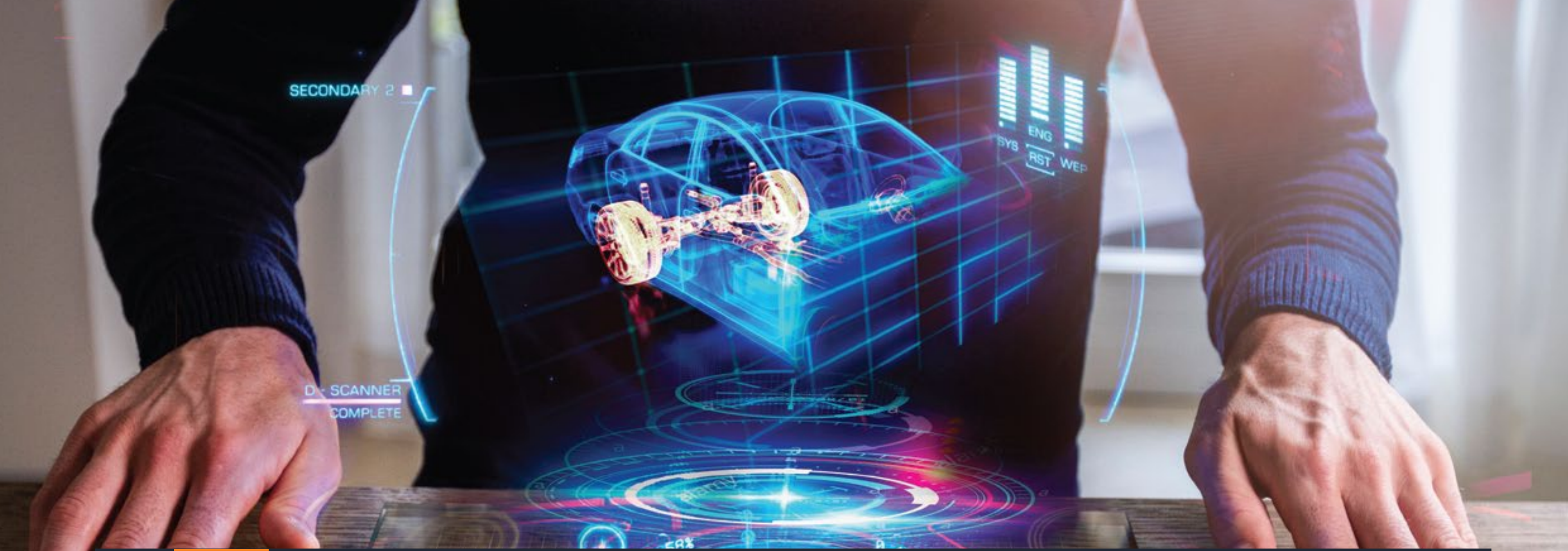
Types of Faults

Systematic

Faults caused by inadequacy in process during design, verification, or manufacturing are systematic faults. They are deterministic and reproducible. Example: A missed or incorrect requirement, incorrect test case. These can be eliminated by adhering to a strict process, for example, ISO 9001. A wrong/missed requirement can be identified during design reviews if we follow the correct approach.

Random

Random HW faults occur unpredictably during the lifetime of a component. This stems from the fact that any HW component will eventually fail for various reasons. Hence, these cannot be eliminated. We can try to detect and prevent it to a certain extent using safety mechanisms.



FMEDA

Failure Mode Effect and Diagnostic Analysis (FMEDA) is a quantitative analysis of the effect of a random hardware fault on a top-level safety goal. We evaluate the effect of the safety mechanisms and their diagnostic coverages on single- and dual-point faults.

The critical point is that the term FMEDA is nowhere mentioned in the ISO 26262 standard. However, we use it to calculate the HW architectural metrics SPFM and LFM.

Inputs/Prerequisites

To perform FMEDA, one needs to understand the safety goal clearly. The HW developer generally does it; however, they need to have a system-level understanding of the safety goal to correctly analyze the impact of each failure mode on safety goal violation. Providing training for Functional Safety from any recognized institute or company internal training is a good start.

From the EE side, schematics and e-BOM are the significant inputs needed.

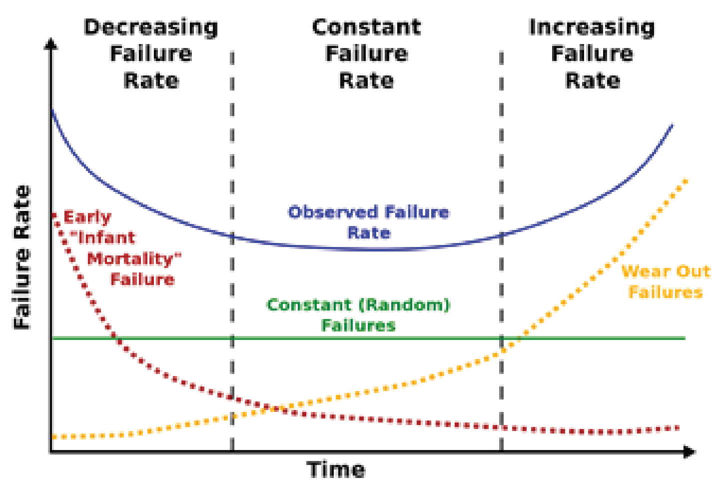
The TSC (Technical Safety Concept) with the safety mechanism is needed from the system side.

The next step is FIT rates and failure modes. One of the ways of getting the failure mode and its distribution is from Alessandro Birolini's Reliability Engineering: Theory and Practice book. We will see below the various methods to calculate the FIT rate.

Failure Rate or Base Failure Rate (BFR)

It is the frequency or rate at which a device or component fails. It is represented by the Greek symbol λ (lambda). The unit of failure rate is FIT (Failure in Time).
1 FIT= 10-9h-1

1 FIT means there is 1 failure in 1 billion operating hours of the component. This means that the product of the number of devices and their operating hours should be 1 billion. So, the FIT rate can be the number of failures in 1 million devices for 1000 operating hours or 1000 devices for 1 million hours.



Failure of electronic components can be modeled in a curve called the bathtub curve. The above bathtub curve consists of three separate regions: Early life, useful life, and wear-out. When we talk about FIT rate, it is the number of failures in the constant failure rate region which is the useful life of the component.

There are various sources for getting the BFR:

1. Recognised Industry standards: Commonly used and recognized standards include SN 29500, IEC 61709, former IEC 62380, MIL HDBK.
2. Tests like High Temperature Operation Lifetime (HTOL) tests
3. Statistics based on field returns
4. Expert judgment

A key point to note here is that all the above sources provide the BFR but with a different confidence level. BFR from industry standards can be considered to have 99% confidence levels. Field return data should have a confidence level of at least 70% if we want to use it in our analysis. Similarly, the HTOL testing data generally has a confidence level of 60% or 70%.

While doing the analysis, we may get the FIT rates from various sources. In such cases, it is necessary to scale the values to an appropriate confidence level. The first edition ISO 26262-5:2011 had a separate annexure, Annex F, which provided an example of scaling factors' application. It has been removed in the 2nd edition. However, the information regarding scaling is still there in many places in the 2nd edition.

FIT rate according to SN 29500

SN 29500 is a lookup table-based standard. It has 16 parts.

Part 1 is general, part2 is for integrated circuits, part 3 is for discrete semiconductors, and part 4 is for passive components. We will not discuss other aspects as they are rarely used in our FIT rate calculations.

The "part2: Expected values for integrated circuits" provides five tables for FIT rates at a reference temperature for different types of ICs. There are separate tables each for memories, microprocessors, digital logic families, analog integrated circuits, and application-specific integrated circuits (ASICs).

These tables provide the base fit rate at a reference condition. To get the FIT rate for our application, the BFR needs to be multiplied by a Voltage dependence factor πU, temperature dependence factor πT, and drift sensitivity factor πD.

$$\lambda = \lambda ref * \pi U * \pi T * \pi D \qquad \text{... Equation 1}$$

Similarly, part 3 provides Base Fit Rates for discrete semiconductors like transistors, diodes, and power semiconductors. Also, we need to apply the relevant factors to get the application-specificFIT rates as discussed above.
Lastly, part 4 provides base fit rates for passive components like various capacitors, resistors, inductors, and other components.

Example: Let us assume we want to calculate the fit rate for a CMOS microprocessor with 600k transistors.

From Table 2 of part 2, SN 29500, we get 80 FIT λref as shown below:

Technology type	No. of gates >100k-1M No. of transistors >500k-5M	Reference temp in °C
CMOS	80 FIT	90

The application FIT rate can be obtained according to equation 1.

2 FIT Rate according to IEC 62380

The IEC 62380 is another commonly used standard for estimating the base failure rate. It was published in 2004 and subsequently withdrawn. However, the contents of IEC62380 related to semiconductors are put in ISO 26262-11:2018 4.6.2.1.1 Model for reliability prediction of electronic components.

The IEC 62380 provides the failure rate of an IC as a sum of the die, package, and electrical overstress (EOS).

The expression for FIT Rate calculation according to IEC TR 62380 and ISO 26262-11:2018 is shown below:

$$\lambda = \left(\underbrace{\left\{ \lambda_1 \times N \times e^{-0{,}35 \times a} + \lambda_2 \right\} \times \left\{ \frac{\sum_{i=1}^{y} (\pi_t)_i \times \tau_i}{\tau_{on} + \tau_{off}} \right\}}_{\lambda_{die}} + \underbrace{\left\{ 2{,}75 \times 10^{-3} \times \pi_\alpha \times \left(\sum_{i=1}^{z} (\pi_n)_i \times (\Delta T_i)^{0{,}68} \right) \times \lambda_3 \right\}}_{\lambda_{package}} + \underbrace{\left\{ \pi_I \times \lambda_{EOS} \right\}}_{\lambda_{overstress}} \right) \times 10^{-9} / h$$

1. The first portion expresses the FIT rate for the die. It contains parameters related to several transistors, the technology used and its maturity, mission profiles
2. The second portion provides the FIT rate for the package. This contains parameters for thermal expansion, package factor, and temperature cycle changes
3. The EOS or the overstress portion has terms for different external interfaces.

We see from the expression that IEC 62380 has a separate FIT rate for die and package. But SN 29500 has no such split. This is a big advantage of using IEC 62380 for FIT rate calculations of Integrated circuits. Below is an example to calculate the FIT rate using this standard.

Example:

Calculate the FIT rate of a microcontroller to be used in Automotive environment with “automotive passenger compartment” mission profile with below details:

Manufacturing year	: 2001
Technology type	: CMOS
Transistor count, N	: 2.5x106
Power dissipated , P	: 0.5W

Rthja : 60 K/W .... from datasheet
Package details : LQFP with 100 pins

Calculation:

λ1 : 3.4x10-6 ... From Table 16 IEC 62380
λ2 : 1.7 ... From Table 16 IEC 62380

Considering natural convection for calculating temperature increase, K=1.4 from Table 13

ΔTj = Rthja x P = 30°C
tj1 = 27 + 30 = 57°C ... Using Mission profile from Table 6
tj2 = 30 + 30 = 60°C ... Using Mission profile from Table 6
tj3 = 85 + 30 = 115°C ... Using Mission profile from Table 6
(πt)1 = e^[A(1/328+1/(273+tj1)] =1.07
(πt)2 = e^[A(1/328+1/(273+tj2)] = 1.17
(πt)3 = e^[A(1/328+1/(273+tj3)] = 5.16
τ1 =0.006 ... Using Mission profile from Table 6
τ2 =0.046 ... Using Mission profile from Table 6
τ3 =0.006 ... Using Mission profile from Table 6
τon+ τoff =1

Package portion

αs = 16 ppm/°C
αc = 21.5 ppm/°C
πa =0.06x(|αs- αc|)1.68=1.05
(tac)1 = (27*0.006+ 30* 0.046 + 85*0.006)/0.058

For an on/off phase ΔTi=[ΔTj/3+(tac)i]-(tae)i

For night starts, tae is 5°C, for day light start tae is 15°C

ΔT1 = (30/3+35) -5 = 40.38
ΔT2 = (30/3+35) -15 = 30.38
ΔT3 = 10
(πn)1 = (670)0.76
(πn)2 = (1340)0.76
(πn)3 = (30)0.76
λ3 = 10.2 FIT ... from Table 17a

Considering no interfaces EOS factor becomes 0

Putting all the values in equation for λ.

λ =
{3.4*10-6*2.5*106*e-0.35*3+1.7}*{(1.07*0.006+1.17*0.046+5.16*0.006)/(0.058+0.942)} +
{2.75*10-3*1.05*(670) 0.76*(40.38)0.68*(1340) 0.76*(30.38)0.68*(30) 0.76*(10)0.68*10.2}
+ {0*λEOS}
= 4.67 + 124.7 FIT
= 129.38 FIT

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FIT Rate calculation according to HTOL tests

JEDEC document JESD85 Methods for Calculating Failure Rates in Units of FITs describes a method for calculating FIT Rates. In this method, a known sample size of the component is stressed to high temperature, for example 125, 135 or 150C. Number of components failing is noted and used in the calculation. Below we have an example of the sample data and FIT rate calculation.

Example:

Test variables

Sample size (ss) = 240

Number of failures (f) = 0

Hours of testing (t) = 1000 hours

Accelerated Temp (Tj) = 145°C

Operating Temp (Tn) = 55°C

Activation Energy (a) = 0.7 eV

Confidence Level (CL) = 60%

Boltzmann's constant (k) = 8.617E-05 eV/K

Calculations

Acceleration factor AF = exp [(Ea/k)*((1/Tn)-(1/Tj))]

= 207

Failure Rate = χ2 (x, v)/(2*t*200*AF)

= 18.45 FIT

Where χ2 is the chi-square value,

x= 1- C.L. and (C.L. = Confidence Level)

v= 2f+2 where f is the number of failures

Conclusion

In the above examples, we saw the various ways of calculating the FIT rates using industry handbooks and HTOL testing. The field return statistics may fail due to systematic and random hardware faults. Hence, this was not included and considered. Another point to keep in mind is to use the same source for calculating the failure rates of all components in the item/system. In cases where multiple sources for failure rates are used, we should ensure that the scaling is done using the appropriate scaling factor.

References

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